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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/778,264	02/07/2001	Chuan-Lin Wu	DEE-PT005	4480

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EXAMINER	
KENDALL, CHUCK O	

ART UNIT	PAPER NUMBER
2122	

DATE MAILED: 08/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/778,264	WU ET AL.	
	Examiner	Art Unit	
	Chuck Kendall	2122	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 February 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the application filed 02/07/01

   Claims 1 - 9 have been examined.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 9 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Applicant has claims to a Motif program. The specification is silent and not descriptive as to what this feature is.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1 & 3 – 8 are rejected under 35 U.S.C. 102(e) as being anticipated by Hellerstrand et al. USPN 6,230,114.

Regarding claim 1, Hellerstrand anticipates a virtual computer verification platform, comprising:

a simulation system (FIG.1) which includes a special function for integrating a microprocessor chip with the simulation system, a concurrent-clock circuit inserted into said microprocessor chip (FIG.1, 110), a peripheral chip simulation subsystem (FIG.1, 111), a peripheral device simulation subsystem (FIG.1, 103) and a bus command compiler (FIG.8, 815); and

a set of on-line debugging auxiliary tools which are connected to said virtual computer simulation system for modifying the contents of said peripheral device to assist said microprocessor chip in debugging (14:25 - 35).

Regarding claim 3, the virtual computer verification platform according to claim 1, wherein said microprocessor chip is coded in a high level hardware description language, Verilog (Hellerstrand,14:35).

Regarding claim 4, the virtual computer verification platform according to claim 1, wherein said special function is vpm_call ( ) written in a C high level programming Language (Hellerstrand, 21:35 – 40) and is used for transferring an interface signal from said microprocessor chip to said peripheral chip simulation subsystem through a message passing mechanism supported by UNIX IPC (Inter-Process Communication) (Hellerstrand, 7:29 –32) and PLI (Programming Language Interface) supported by Verilog (Hellerstrand,15: 25 –35, see PLI and Verilog).

Regarding claim 5, the virtual computer verification platform according to claim 4, wherein said concurrent-clock circuit is used for creating a synchronic clock between

said simulation system and said microprocessor chip (Hellerstrand, 8:47 – 57), collecting said interface signal from said microprocessor in each clock cycle, delivering said special function into said simulation system beyond said microprocessor chip in a leading edge and a trailing edge of each synchronic clock cycle, and waiting for a result to achieve synchronic transfer and data transfer (Hellerstrand, 8:53 - 9:12, see synchronize also see timing information for cycle).

Regarding claim 6, the virtual computer verification platform according to claim 1, wherein said peripheral chip simulation subsystem is used for integrating each individual virtual peripheral chip and is designed in terms of an object-oriented programming technology (Hellerstrand, 25: 55, show "C" which is an object oriented language) for providing a peripheral control chipset of the simulation system with performance, interface protocol and clock (Hellerstrand, 26: 5 – 25, for integration see assembly).

Regarding claim 7, the virtual computer verification platform according to claim 1, wherein said peripheral device simulation subsystem is used for integrating individual virtual peripheral device and is designed in terms of an object-oriented programming technology for providing a peripheral device of the simulation system with performance (Hellerstrand, 7: 57 – 67, see accommodate addition processor).

Regarding claim 8, the virtual computer verification platform according to claim 1, wherein said bus command compiler is used for compiling a protocol signal command from said microprocessor chip and transferring a compiled command into said peripheral chip simulation subsystem (Hellerstrand 5:45 – 55).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hellerstrand et al. USPN 6,230,114 as applied in claim 1, in view of Zaidi US 20020038401 A1.

Regarding claim 2, Hellerstrand discloses all the claimed limitations as applied in claims 1 above including the virtual computer verification platform according to claim 1, wherein said microprocessor chip is designed in a Behavior model (11:66). Although Hellerstrand doesn't explicitly disclose a RTL and a Gate model he does disclose using Verilog, as the preferred HDL (14:35) which generally uses RTL source code as disclosed in Zaidi [0033]. Zaidi in an analogous prior art disclcose in [0039], and inclusion of " RTL source code for commonly used design components. These modules are written in synthesizable Verilog or VHDL and are referenced by the various block design embodiments", as well as Gate models were he also notes in [0066] that "gate level simulations can be run on the design once it has been synthesized successfully into a complete chip Verilog gate level netlist". Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Hellerstrand and Zaidi because, RTL is a commonly used in Verilog and would make the invention more compatible.

Correspondence Information

8. Any inquires concerning this communication or earlier communications from the examiner should be directed to Chuck O. Kendall who may be reached via telephone at (703) 308-6608. The examiner can normally be reached Monday through Friday between 8:00 A.M. and 5:00 P.M. est.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Dam *can be* reached at *(703) 305-4552.*

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is *(703) 305-3900.*

For facsimile (fax) send to 703-7467239 official and 703-7467240 draft

Chuck O. Kendall

Software Engineer Patent Examiner

WEI Y. ZHEN
PRIMARY EXAMINER